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EXAMINER	
DAY, HERNG DER	

ART UNIT	PAPER NUMBER
2128	

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8

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/531,910	YADAVALLI ET AL.	
	Examin r	Art Unit	
	Herng-der Day	2128	

-- The MAILING DATE of this communication appears on the c ver sheet with the corresp ndence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 October 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This communication is in response to Applicants' Amendment and Response (paper # 6) to Office Action dated July 16, 2003 (paper # 4), mailed October 23, 2003, and received by PTO October 27, 2003.

1-1. Claims 1-21 have been cancelled; claims 22-39 have been added; claims 22-39 are pending.

1-2. Claims 22-39 have been examined and claims 22-39 have been rejected.

Drawings

2. The proposed drawing corrections to Fig. 3A and Fig. 4 received by PTO on October 27, 2003, have been approved. However, according to the added new claims, the drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. For example, the "providing a virtual clock signal to the virtual delay element" and "generating a test pattern to test the circuit" must be shown or the features canceled from the claims. No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

3. All the amended paragraphs of the specification are approved. The objection to the specification has been withdrawn.

Claim Objections

4. Applicants have cancelled claims 1-21. The objection to the claims has been withdrawn.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 22-39 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

6-1. All the Applicants' newly added independent claims 22, 28, and 34 recite the limitation "identifying a race condition in a circuit" or "identify a race condition in a circuit". It does not appear to have support in the original disclosure. In the original disclosure, examples under presumed conditions are given to illustrate the well-known min-delay problem, however, how to "identify a race condition in a circuit" has not been disclosed. Therefore, without undue experiment, it is unclear for one skilled in the art how to make and/or use the claimed invention.

Claims 23-27, 29-33, and 35-39 are rejected as being dependent on their rejected independent claims.

6-2. Applicants' newly added claims 25, 31, and 37 recite the limitation "with a physical characteristic of the circuit". It does not appear to have support in the original disclosure. As described in lines 10-12 of page 8, only "exact delay characteristics of the physical circuit" has been disclosed. Therefore, without undue experiment, it is unclear for one skilled in the art how to specify the virtual clock signal in accordance with a physical characteristic of the circuit. Claims 26-27, 32-33, and 38-39 are rejected as being dependent on their respectively rejected claims.

6-3. Applicants' newly added claims 27, 33, and 39 recite the limitation "the delay characteristic corresponds to a length of conductive paths between circuit elements". It does not appear to have support in the original disclosure. As described in lines 10-12 of page 8, only "exact delay characteristics of the physical circuit" has been disclosed. Therefore, unless it is well known, "the delay characteristic corresponds to a length of conductive paths between circuit elements" has no support in the original disclosure.

7. Claims 23, 29, and 35 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7-1. Claims 23 and 35 recite the limitation "selectively providing a virtual delay element for respective sequential elements in the circuit" and claim 29 recites the limitation "selectively provide a virtual delay element for respective sequential elements in the circuit". However, the

original specification has not disclosed how, or based on what criteria, to *selectively* provide *a* virtual delay *element* for respective *sequential elements* in the circuit. Therefore, without undue experiment, it is unclear for one skilled in the art how to make and/or use the claimed invention.

Claim Interpretation

8. Independent claims 22, 28, and 34 recite the limitation "identifying a race condition in a circuit" or "identify a race condition in a circuit". It does not appear to have support in the original disclosure, as detailed in section **6-1** above. For the purpose of claim examination with the broadest reasonable interpretation, the Examiner will interpret that the limitation "identifying a race condition in a circuit" or "identify a race condition in a circuit" is the teaching of Zeiner et al., in U.S. Patent, 5,798,645, "By the programmable delay units, race problems can be detected" (Abstract).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 22-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zeiner et al., U.S. Patent 5, 798,645 issued August 25, 1998, in view of Selvidge et al., U.S. Patent 5,649,176 issued July 15, 1997, and further in view of Dargelas, U.S. Patent 5, 938,785 issued August 17, 1999.

10-1. Regarding claim 22, Zeiner et al. disclose a method, comprising:

identifying a race condition in a circuit (race problems can be detected, Abstract);

generating a netlist model for the circuit (a netlist 14 is established, column 5, lines 13-31; and FIG. 2);

Zeiner et al. fail to expressly disclose providing a virtual delay element and a virtual clock signal. Nevertheless, Zeiner et al. suggest inserting programmable delay units in each logic cell (column 3, lines 20-30) and providing the signal lines of the free-programmable coupling fields with adjustable delay elements (column 4, lines 27-31) in order to take into account the time behavior of the circuit to be designed.

Selvidge et al. disclose using a digital circuit description to generate the resynthesized circuit and the result is a logic netlist of the resynthesized circuit including the new circuit elements and the new VClk (Selvidge, column 20, lines 8-13). Specifically, Selvidge et al. disclose:

providing a virtual delay element in the netlist model (Selvidge, flip-flop 1602 in FIG. 16B; and column 18, lines 58-63);

providing a virtual clock signal to the virtual delay element to influence a desired race resolution for the circuit ((Selvidge, virtual clock VClk in FIG. 16B; and column 18, lines 58-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Zeiner et al. to incorporate the teachings of Selvidge et al. to obtain the invention as specified in claim 22 because the virtual delay element and the virtual

clock signal disclosed by Selvidge et al. is the detailed implementation of the programmable delay unit, which is suggested by Zeiner et al.

Zeiner et al. also fail to expressly disclose generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element. Nevertheless, Zeiner et al. do suggest using a test pattern to detect all possible fault sources (Zeiner, column 7, lines 19-21).

Dargelas discloses automatically determining test patterns for a netlist having multiple clocks and sequential circuits (Dargelas, Abstract). Specifically, Dargelas discloses:

generating a test pattern to test the circuit in accordance with the virtual clock signal for the virtual delay element (Dargelas, Abstract).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combined teachings of Zeiner et al. and Selvidge et al. to incorporate the teachings of Dargelas to obtain the invention as specified in claim 22 because Dargelas discloses automatically determining test patterns for a netlist having multiple clocks and sequential circuits as suggested by Zeiner et al.

10-2. Regarding claim 23, Selvidge et al. further disclose comprising:

providing a virtual delay element for respective sequential element in the circuit in accordance with respective race resolution requirements of the respective sequential element (Selvidge, flip-flop 1602 in FIG. 16B; and column 18, lines 58-63).

10-3. Regarding claim 24, Dargelas further discloses the virtual clock signal is identified as a primary input of an automatic test pattern generation (ATPG) system (Dargelas, the multiple clock signals are primary input clock signals, column 6, lines 25-27).

10-4. Regarding claim 25, Selvidge et al. further disclose the virtual clock signal is specified by a user of the ATPG system in accordance with a physical characteristic of the circuit (Selvidge, virtual clock cycles are required for the values in the loop to settle into their final states, column 18, lines 65-67).

10-5. Regarding claim 26, Selvidge et al. further disclose the physical characteristic comprises a delay characteristic (Selvidge, delay period and clock cycles to settle, column 19, lines 1-14).

10-6. Regarding claim 26, Selvidge et al. further disclose the delay characteristic corresponds to a length of conductive paths between circuit elements (Selvidge, cycles are nested, column 19, lines 1-14).

10-7. Regarding claims 28-33, these system claims include same method limitations as in claims 22-27 and are unpatentable using the same analysis of claims 22-27.

10-8. Regarding claims 34-39, these medium claims include same method limitations as in claims 22-27 and are unpatentable using the same analysis of claims 22-27.

Applicants' Arguments

11. Applicants argue in page 8 of paper # 6, "Applicants have canceled claims 1-21, rendering these rejections moot".

Response to Arguments

12. Applicants' argument has been fully considered and are persuasive. Therefore, the original claim rejections under 35 U.S.C. 112, second paragraph, for indefiniteness have been

withdrawn. Also, the rejections of claims 1-21 under 35 U.S.C. 102(b) and 103(a) in paper # 4 have been withdrawn.

Conclusion

13. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Herng-der Day whose telephone number is (703) 305-5269. The examiner can normally be reached on 9:00 - 17:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (703) 305-9704. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Herng-der Day
January 11, 2004

HUGH JONES Ph.D.
PRIMARY PATENT EXAMINER
TECHNOLOGY CENTER 2100